PRELIMINARY
November 2009

AR7241: A High Performance And Cost-Effective Network Processor

General Description

The Atheros AR7241 is a high performance and cost effective network processor for access point, router, and gateway applications. It includes a MIPS 24K processor, PCI Express host interface, integrated 802.3 Ethernet Switch with five 10/100 Mbps Fast Ethernet MAC/PHY, one USB 2.0 MAC/PHY, and external memory interface for serial Flash, DDR1 or DDR2 interface, an I^2S audio interface, a high-speed UART, and GPIOs that can be used for LED controls or other general purpose interface configurations.

The AR7241 is a memory-centric architecture including various DMA controlled interfaces that access the DDR memory.

The AR7241 network processor, when paired with the AR9287 single chip 802.11n MAC/BB/Radio family, provides the best-in-class WLAN solution capable of supporting 802.11b/g/n standards.

Features

- Integrated MIPS 24 K 32-bit processor operating at up to 400 MHz
- 64 K instruction cache and 32 K data cache
- Integrated Ethernet Switch with four 10/100 802.3 Ethernet LAN ports and one WAN port
- 16-bit DDR1 or DDR2 memory interface supporting up to 400 M transfers per second
- An external serial Flash memory interface (maximum 16 MBytes)
- One USB 2.0 controller with built-in MAC/PHY support
- High-speed UART and multiple GPIO pins for general purpose I/O or LED control
- A single lane PCI Express 1.1 interface that can be used for interfacing to the AR9287 single chip 802.11n MAC/BB/Radio
- JTAG port support for processor core
- 14 mm x 14 mm 128-pin LQFP lead-free package

System Block Diagram

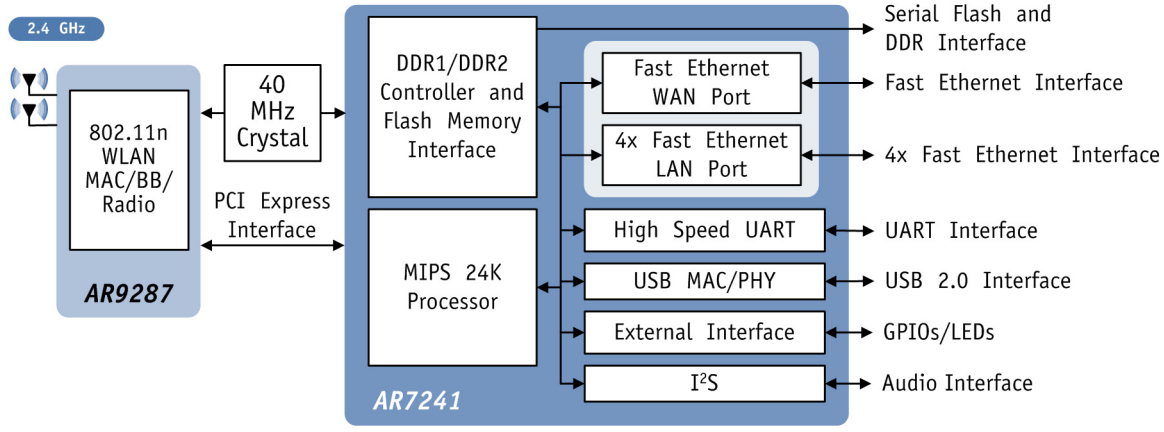


Table of Contents

1. Pin Descriptions

This section contains a package pinout (see Figure 1-1 and Table 1-2) and a tabular listing of the signal descriptions.

This nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

This nomenclature is used for signal types:

I	Digital input signal
I/O	A digital bidirectional signal
IA	Analog input signal
IA/OA	Analog bidirectional signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
O	A digital output signal
OA	An analog output signal
OD	A digital output signal with open drain
P	A power or ground signal

Figure 1-1 shows the LQFP-128 AR7241 pinout.

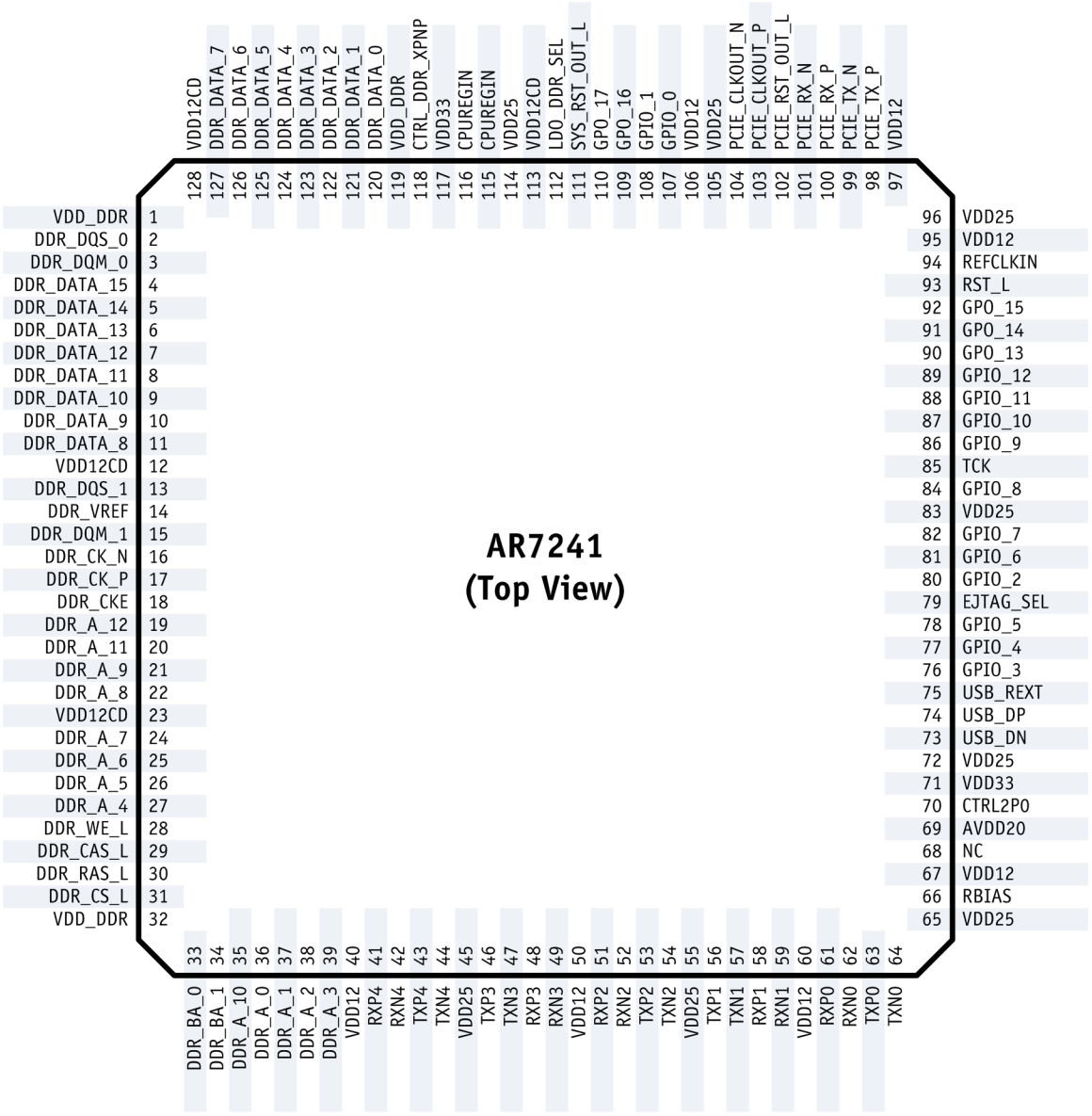


Figure 1-1. **LQFP-128 Package Pinout**

Table 1-1 shows the multiplexed pins for the AR7241,

Table 1-1. **Multiplexed Pins[1][2]**

LQFP-128 Pin	GPIO Pin	EJTAG Pin	LED Pin	SPDIF/I²S Pin	SPI Pin	UART Pin
107	GPIO_0			I2S_WS (FN2, 4)	SPI_CS_1 (FN1, 14)	
108	GPIO_1			I2S_CK (FN2, 3)	SPI_CS_2 (FN1, 13)	
80	GPIO_2				SPI_CS_0 (FN1, 18)	
76	GPIO_3				SPI_CLK (FN1, 18)	
77	GPIO_4				SPI_MOSI (FN1, 18)	
78	GPIO_5				SPI_MISO (FN1, 18)	
81	GPIO_6	TDI[3] (FN1, 0)		I2S_CK (FN1, 26)		
82	GPIO_7	TDO[3] (FN1, 0)		I2S_WS (FN1, 26)		
84	GPIO_8	TMS[3] (FN1, 0)		I2S_SD (FN1, 26)		
86	GPIO_9					UART_SIN (FN1, 1)
87	GPIO_10					UART_SOUT (FN1, 1)
88	GPIO_11			I2S_MCK (FN1, 26, 27)		UART_RTS (FN1, 2)
89	GPIO_12			I2S_MICIN (FN1, 26) I2S_SD (FN2, 5)		UART_CTS (FN1, 2)
90	GPO_13		LED_0 (FN1, 3)	SPDIF_OUT (FN1, 30)		
91	GPO_14		LED_1 (FN1, 4)	I2S_SD (FN2, 1)		
92	GPO_15		LED_2 (FN1, 5)	I2S_WS (FN2, 1)		
109	GPO_16		LED_3 (FN1, 6)	I2S_CK (FN2, 1)		
110	GPO_17		LED_4 (FN1, 7)			
85	GPIO_18	TCK[3] (FN1, 0)		SPDIF_OUT (FN1, 30, 31)		
79	GPIO_19	EJTAG_SEL[3] (FN1, 0)				

[1]Multiplexing of the GPIO pins is controlled by the registers "GPIO Function (GPIO_FUNCTION_1)" on page 50 and "Extended GPIO Function Control (GPIO_FUNCTION_2)" on page 51.

[2]Notations of (FN*x*, *y*) indicate that the pin is controlled by the particular register and bit. For example, (FN1, 30, 31) indicates the "GPIO Function (GPIO_FUNCTION_1)" register, bit [30] and bit [31], and (FN2, 1) indicates the "Extended GPIO Function Control (GPIO_FUNCTION_2)" register, bit [1].

[3]The EJTAG interface is enabled by default. To use the EJTAG interface as GPIO pins, the JTAG_DISABLE bit in the "GPIO Function (GPIO_FUNCTION_1)" register must be set to 1.

Table 1-2. **Signal-to-Pin Relationships and Descriptions**

Symbol	LQFP-128 Pin	Type	Description
Reset and Clock			
REFCLKIN	94	I	40 MHz reference clock input, AC coupled, can be sine wave or square wave. An external 100 pF capacitor should connect between REFCLKIN and the clock source. See Table 4-7 and Table 4-8 on page 32 for more information.
RST_L	93	IH	Power on reset with internal weak pull-up. Refer to reference design schematics
SYS_RST_OUT_L	111	OD	System reset out, open drain, pull up is required
PCI Express			
PCIE_CLKOUT_N	104	OA	Differential reference clock (100 MHz)
PCIE_CLKOUT_P	103	OA	
PCIE_RST_OUT_L	102	OD	PCI Express reset, open drain
PCIE_RX_N	101	IA	Differential receive
PCIE_RX_P	100	IA	
PCIE_TX_N	99	OA	Differential transmit
PCIE_TX_P	98	OA	
Serial Interface			
SPI_CLK[1]	76	O	Serial interface clock
SPI_CS_0[1]	80	O	SPI chip select
SPI_CS_1[1]	107	O	
SPI_CS_2[1]	108	O	
SPI_MOSI[1]	77	O	Data transmission from the AR7241 to an external device. On reset, SPI_MISO (GPIO_5) is input and SPI_MOSI (GPIO_4) is output so it can directly interface with a SPI device such as a serial flash. If a serial flash is not used, these pins may be used as GPIO pins.
SPI_MISO[1]	78	IL	Data transmission from an external device to the AR7241. On reset, SPI_MISO (GPIO_5) is input and SPI_MOSI (GPIO_4) is output so that it can directly interface with a SPI device such as a serial flash. If a serial flash is not used, these pins may be used as GPIO pins.
USB			
USB_DM	73	IA/OA	USB 2.0 D- data pin
USB_DP	74	IA/OA	USB 2.0 D+ data pin
USB_REXT	75	IA/OA	Connect to external 6.04 KΩ resistor
UART			
UART_CTS[1]	89	I	UART clear to send signal
UART_RTS[1]	88	O	UART ready to send signal (optional UART interface pin)
UART_SIN[1]	86	I	Serial data in

Table 1-2. **Signal-to-Pin Relationships and Descriptions (continued)**

Symbol	LQFP-128 Pin	Type	Description
UART_SOUT[1]	87	O	Serial data out
DDR			
DDR_BA_0	33	O	DDR bank address
DDR_BA_1	34	O	
DDR_CS_L	31	O	DDR chip select
DDR_CK_N	16	O	DDR clock
DDR_CK_P	17	O	
DDR_CKE	18	O	DDR clock enable
DDR_DQM_0	3	O	DDR data mask
DDR_DQM_1	15	O	
DDR_DQS_0	2	I/O	DDR data strobe In DDR2, both polarity signals need to be driven.
DDR_DQS_1	13	I/O	
DDR_CAS_L	29	O	DDR column address strobe
DDR_RAS_L	30	O	DDR row address strobe
DDR_WE_L	28	O	DDR write enable
DDR_VREF	14	I	DDR reference level for SSTL signals
DDR_A_0	36	O	DDR address
DDR_A_1	37	O	
DDR_A_2	38	O	
DDR_A_3	39	O	
DDR_A_4	27	O	
DDR_A_5	26	O	
DDR_A_6	25	O	
DDR_A_7	24	O	
DDR_A_8	22	O	
DDR_A_9	21	O	
DDR_A_10	35	O	
DDR_A_11	20	O	
DDR_A_12	19	O	

Table 1-2. **Signal-to-Pin Relationships and Descriptions (continued)**

Symbol	LQFP-128 Pin	Type	Description
DDR_DATA_0	120	I/O	DDR data bus
DDR_DATA_1	121	I/O	
DDR_DATA_2	122	I/O	
DDR_DATA_3	123	I/O	
DDR_DATA_4	124	I/O	
DDR_DATA_5	125	I/O	
DDR_DATA_6	126	I/O	
DDR_DATA_7	127	I/O	
DDR_DATA_8	11	I/O	
DDR_DATA_9	10	I/O	
DDR_DATA_10	9	I/O	
DDR_DATA_11	8	I/O	
DDR_DATA_12	7	I/O	
DDR_DATA_13	6	I/O	
DDR_DATA_14	5	I/O	
DDR_DATA_15	4	I/O	
LED			
LED_0[1]	90	OD	If ETH_SWITCH_LED0_EN is set, it becomes open drain and provides drive strength of 10 mA
LED_1[1]	91	OD	If ETH_SWITCH_LED1_EN is set, it becomes open drain and provides drive strength of 10 mA
LED_2[1]	92	OD	If ETH_SWITCH_LED2_EN is set, it becomes open drain and provides drive strength of 10 mA
LED_3[1]	109	OD	If ETH_SWITCH_LED3_EN is set, it becomes open drain and provides drive strength of 10 mA
LED_4[1]	110	OD	If ETH_SWITCH_LED4_EN is set, it becomes open drain and provides drive strength of 10 mA

Table 1-2. **Signal-to-Pin Relationships and Descriptions (continued)**

Symbol	LQFP-128 Pin	Type	Description	
JTAG				
EJTAG_SEL	79	I	0	JTAG
			1	EJTAG (enhanced JTAG)
TCK[1]	85	I	JTAG/EJTAG clock	
TDI[1]	81	I	JTAG/EJTAG data input	
TDO[1]	82	O	JTAG/EJTAG data output	
TMS[1]	84	I	JTAG/EJTAG mode select	
Ethernet				
RBIAS	66	OA	Connect to 2.37 KΩ resistor to ground	
RXN0	62	IA/OA	Port 0	
RXP0	61	IA/OA		
TXN0	64	IA/OA		
TXP0	63	IA/OA		
RXN1	59	IA/OA	Port 1	
RXP1	58	IA/OA		
TXN1	57	IA/OA		
TXP1	56	IA/OA		
RXN2	52	IA/OA	Port 2	
RXP2	51	IA/OA		
TXN2	54	IA/OA		
TXP2	53	IA/OA		
RXN3	49	IA/OA	Port 3	
RXP3	48	IA/OA		
TXN3	47	IA/OA		
TXP3	46	IA/OA		
RXN4	42	IA/OA	Port 4	
RXP4	41	IA/OA		
TXN4	44	IA/OA		
TXP4	43	IA/OA		

Table 1-2. **Signal-to-Pin Relationships and Descriptions (continued)**

Symbol	LQFP-128 Pin	Type	Description
GPIO			
GPIO_0[1]	107	I/O	General purpose input/output with drive strength of 2 mA.
GPIO_1[1]	108	I/O	
GPIO_2[1]	80	I/O	
GPIO_3[1]	76	I/O	
GPIO_4[1]	77	I/O	
GPIO_5[1]	78	I/O	
GPIO_6[1]	81	I/O	GPIO pin multiplexed as TDI by default
GPIO_7[1]	82	I/O	GPIO pin multiplexed as TDO by default
GPIO_8[1]	84	I/O	GPIO pin multiplexed as TMS by default
GPIO_9[1]	86	I/O	General purpose input/output with drive strength of 2 mA.
GPIO_10[1]	87	I/O	
GPIO_11[1]	88	I/O	
GPIO_12[1]	89	I/O	
GPO_13[1]	90	O	These pins are intended for driving Ethernet LEDs and cannot be used as inputs. See the pin descriptions for "LED" on page 10.
GPO_14[1]	91	O	
GPO_15[1]	92	O	
GPO_16[1]	109	O	
GPO_17[1]	110	O	
GPIO_18[1]	85	I/O	GPIO pin multiplexed as TCK by default
GPIO_19[1]	79	I/O	GPIO pin multiplexed as EJTAG_SEL by default
I^2S/SPDIF			
I2S_CK[1]	81, 108, 109	O	Stereo clock
I2S_MCK[1]	88	O	Master clock
I2S_MICIN[1]	89	I	Data input
I2S_SD[1]	84, 89, 91	I/O	Serial data input/output
I2S_WS[1]	82, 92, 107	O	Word select for stereo
			0 Right
			1 Left
SPDIF_OUT[1]	85, 90	O	Speaker output

[1]This pin is multiplexed. See Table 1-1.

Symbol	Pin	Description	
Regulator Control			
CPUREGIN	115, 116	I	CPU regulator control inputs. Minimum voltage is 1.8 V. A 1 Ω resistor may be used in series between these pins and VDD_DDR pins in DDR1 mode (LDO_DDR_SEL=1).
CTRL_DDR _XPNP	118	OA	External PNP Control. Connect to the base of an external PNP: collector to VDD_DDR and emitter to VDD33.
CTRL2P0	70	OA	External PNP control. Connect to the base of an external PNP: collector to AVDD20 and emitter to VDD33.
LDO_DDR_SEL	112	I	Selects the regulated DDR voltage, see VDD_DDR description
		0	DDR2 voltage, 1.8 V
		1	DDR1 voltage, 2.6 V
Power			
AVDD20	69	Regulated 2.0 V from the AR7241; connect to the external PNP collector.	
VDD_DDR	1, 32, 119	Regulated 2.6 V or 1.8 V output from the AR7241, for DDR1 or DDR2, respectively. Connect to the external PNP collector.	
VDD12	40, 50, 60, 67, 95, 97, 106	Regulated 1.2 V output from the AR7241	
VDD12CD	12, 23, 113, 128	Regulated 1.28 V output from the AR7241; core voltage of CPU/ DDR blocks, connect pins 12 and 23 to pins 113 and 128	
VDD25	45, 55, 65, 72, 83, 96, 105, 114	Regulated 2.62 V output from the AR7241; I/O voltage	
VDD33	71, 117	3.3 V power supply	
Ground Pad			
Exposed Ground Pad		Tied to GND (see "Package Dimensions" on page 36)	
No Connection			
NC	68	No connection	

2. System Architecture

Figure 2-1 illustrates the AR7241 system architecture.

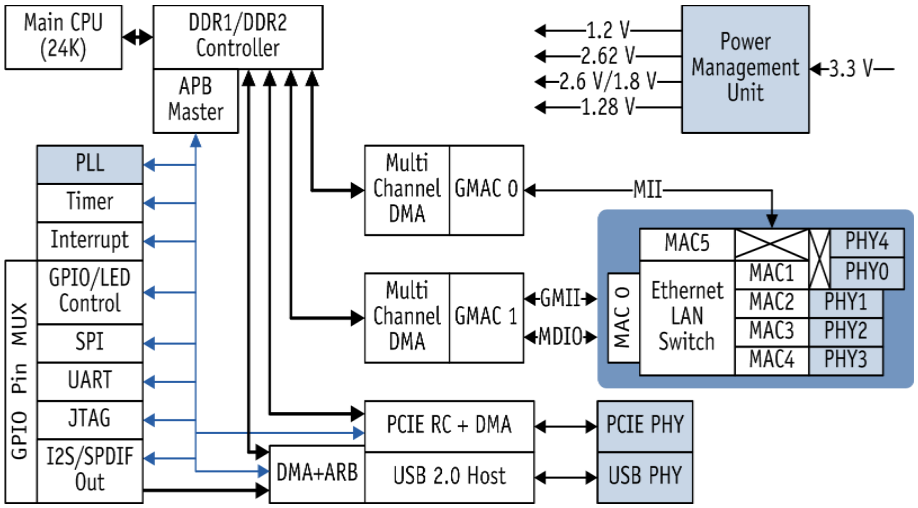


Figure 2-1. **AR7241 Functional Block Diagram**

Table 2-1 summarizes the functional blocks that comprise the AR7241.

Table 2-1. **Functional Block Descriptions**

Block	Description
CPU	This MIPS 24 K processor can run up to 400 MHz. It includes a 64 K 4-way set associative instruction cache, 32 K 4-way set associative data cache, single cycle multiply-accumulate, and MIPS32 and MIPS16 instruction sets. Non-blocking cache reads are also supported. See "MIPS Processor" on page 16.
DDR Memory Controller	The AR7241 supports a 16-bit DDR1/ DDR2 memory interface of up to 400Mbps/pin. It supports one dedicated point-to-point interface for the CPU and similarly dedicated point-to-point interfaces for the USB, Ethernet and PCIE master devices. See "DDR Memory Controller" on page 17.
Ethernet Switch/ GMAC	Four LAN ports and one WAN port with integrated PHY. LED indication for each port is supported. The four LAN ports connect to the CPU through the GE1 GMII interface, and four Tx queue priorities are supported in each LAN port. The WAN port connects to the CPU using the GE0 MII interface. The MII interface can support up to four priority queues, with either simple priority or a weighted round robin arbitration mechanism. Switch functions such as QoS and VLAN are supported.
Bus Bridge	High speed peripheral bus; the APB connects peripherals such as GPIO, UART, and SPI for Flash to the bus bridge. The AHB connects high-performance peripheral interfaces such as the GB Ethernet and USB interfaces to the bus bridge. See "AHB Master Bus" on page 17 and "APB Bridge" on page 17.
GPIO	20 multiplexed GPIO pins: 5 of which are output-only intended for driving LEDs, the others can be used for general purpose controls, SPI, I^2S, SPDIF, and UART. See Table 1-1 on page 7 for GPIO multiplexing.

Table 2-1. **Functional Block Descriptions (continued)**

I^2S/ SPDIF	AR7241 audio support consists of: ■ I^2S/SPDIF out audio interface that support up to 48 KHz sampling clock and a serial clock of more than 512 * sampling frequency. It also supports seamless switching of the audio out stream from I2S to SPDIF. I2S MIC is also supported. ■ A dedicated audio PLL to generate serial clock for various sampling frequencies. See "Audio Interface" on page 25.
PCIE	The root complex single lane interface can support up to 2.56 Gbps and supports both the message-based and MSI interrupt mechanism.
PLL	The PLL block consists of six PLLs used to generate: ■ A clock for CPU/DDR, tunable from 300 MHz to 450 MHz ■ PLL for 48 MHz reference clock for the USB core and to generate a 25 MHz reference clock for the Ethernet Switch ■ PCIE 100 MHz clocks with dither support ■ PCIE PHY PLL generates 250 MHz and 2.5 GHz clock for the PCIE interface ■ Ethernet 125 MHz clock generated from a 25 MHz clock ■ PLL to generate the master clock for I^2S/SPDIF out
SPI	SPI interface that can be used for serial Flash.
UART	16650 equivalent UART for debug/console
USB	Universal Serial Bus 2.0 host interface support.

2.1 MIPS Processor

The AR7241 integrates an embedded MIPS 24Kc processor. For complete information on the 24Kc processor, visit: http://www.mips.com/products/cores/32-bit_cores/MIPS32_24K_Family.php#

Under Processor Cores-24K Family, refer to:

- MIPS32 24Kc Processor Core Datasheet v3.04
- MIPS32 24Kc Processor Core Family Software User's Manual v3.05

Under EJTAG, refer to:

- EJTAG Specification v2.60

2.2 Configuration

Table 2-2 summarizes the configuration settings used by the AR7241. Upon reset, the CPU puts out an address of 0xBFC00000 which is mapped to the flash address space.

The AR7241 processor supports a clock frequency of up to 400 MHz.

Table 2-2. **Core Processor Configuration Settings**

Setting	Description
Cache Size	The AR7241 implements 64 KB 4-way set associative instruction cache and 32 KB four-way set associative data cache. It supports single cycle multiply-accumulate, MIPS32 and MIPS16 instruction sets and non-blocking cached reads.
Endian	The AR7241 implements big Endian addressing.
Block Addressing	The AR7241 implements sequential ordering.

2.3 AR7241 Address MAP

The address space for the AR7241 is divided into two 256 MBytes (MB) regions. The lower region maps to the DDR memory. The upper region maps to the AHB bus bridge. The 512 MBytes decoded region is repeated through the 4 GBytes of the processor's address space. Figure 2-2 shows the address space allocation.

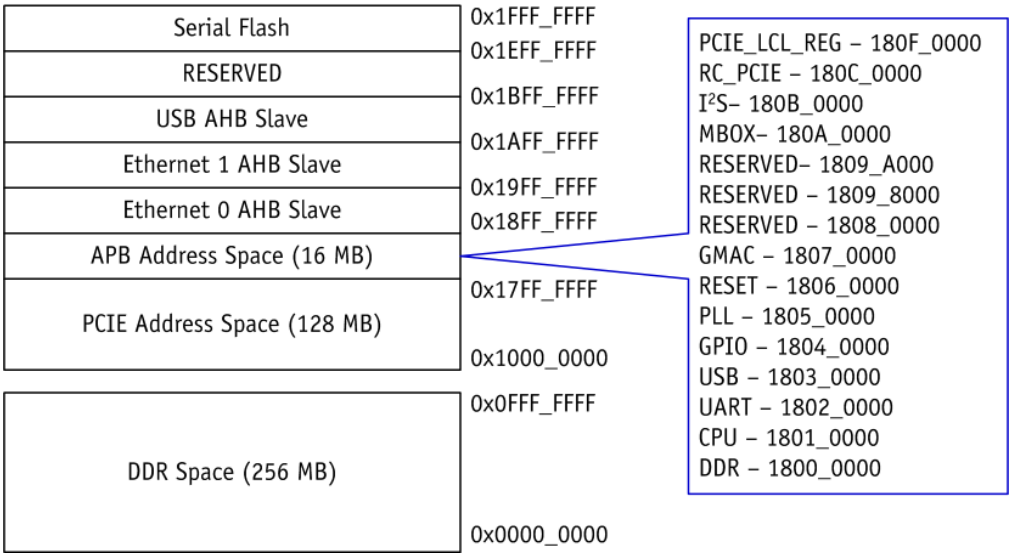


Figure 2-2. **Address Space Allocation**

2.4 AHB Master Bus

The 256 MByte region of address space for the AHB devices is divided into two major windows, 128 MByte for the PCIE and the remainder for the internal DDR AHB master interfaces such as APB, GE0, GE1, and serial flash.

2.5 APB Bridge

One 16 MByte window of the AHB address space is devoted to an APB device mapper. The APB space contains the register address spaces of most of the interfaces, including PCIE, serial flash, GPIO, and UART. This space also provides access to the watchdog timer and four general purpose timers.

2.6 DDR Memory Controller

The AR7241 supports a 16-bit DDR1/DDR2 memory interface of up to 64 MBytes of memory in a single device. It supports one dedicated point-to-point interface for the CPU and similarly dedicated point-to-point interfaces for the CPU, USB, Ethernet and PCIE master devices. Write transactions are buffered at each interface. It implements separate arbitration for each bank thus allowing efficient pipelined RAS/CAS/precharge scheduling.

The DDR block has five AHB-slave interfaces for: GE0, GE1, USB, PCIE, and CPU. External DDR is powered by the AR7241 using an external power transistor. Depending on the LDO_DDR_SEL input, the AR7241 internal regulator generates VDD_DDR output voltage to power the external DDR memory. Table 2-3 shows the LDO_DDR_SEL configurations.

Table 2-3. **LDO_DDR_SEL Voltage Configuration**

LDO-DDR_SEL Input	DDR Voltage	Device Type
0	1.8 V	DDR2
1	2.6 V	DDR1

See Figure 4-1, "Output Voltages Regulated by the AR7241," on page 33.

Table 2-4 shows the DDR configurations.

Table 2-4. **DDR Configurations**

Device Type/Total Cap.	Device Count	Device Type
128 MB (8 M x 16)	1	DDR1
256 MB (16 M x 16)	1	DDR1
256 MB (16 M x 16)	1	DDR2
512 MB (32 M x 16)	1	DDR2

Table 2-5 shows the correspondence of the internal CPU address, the DDR interface address, and the physical memory address.

Table 2-5. **Address Mapping**

CPU Address Bit	AR7241 DDR Interface Address	Corresponding 16-bit DDR Memory Address[1]
0	DDR_A_0, Unused (x16 DRAM)	
1	DDR_A_1	CAS0
2	DDR_A_2	CAS1
3	DDR_A_3	CAS2
4	DDR_A_4	CAS3
5	DDR_A_5	CAS4
6	DDR_A_6	CAS5
7	DDR_A_7	CAS6
8	DDR_A_8	CAS7
9	DDR_A_9	CAS8
10	DDR_A_0	RAS0
11	DDR_BA_0	BA0
12	DDR_BA_1	BA1
13	DDR_A_1	RAS1
14	DDR_A_2	RAS2
15	DDR_A_3	RAS3
16	DDR_A_4	RAS4
17	DDR_A_5	RAS5
18	DDR_A_6	RAS6
19	DDR_A_7	RAS7
20	DDR_A_8	RAS8
21	DDR_A_9	RAS9
22	DDR_A_10	RAS10
23	DDR_A_11	RAS11
24	DDR_A_12	RAS12
25	DDR_A_11	CAS9
26	DDR_A_12	CAS11

[1]CAS10 is a precharge bit, typically 0.

2.7 Serial Flash (SPI)

The single SPI chip select is dedicated to an external flash to boot the chip. Two configurable chip selects are available to bit-bang using GPIOs that configure external components. As an AHB slave, the SPI controller only supports word transactions. Because serial flash supports cached reads (but not cached writes) functionality, the CPU must perform uncached write, but a read can be accelerated by performing cached reads. By default, the REMAP_DISABLE bit is zero which only 4 MBytes are accessible. By setting this bit to 1, up to 16 MBytes of flash space can be accessed.

2.8 UART

The AR7241 contains a single 16550 equivalent UART port for debug/console. The UART pins are multiplexed with GPIO pins, therefore the "GPIO Function (GPIO_FUNCTION_1)" register bits control which GIPIO pins are used for UART functions.

2.9 GE0 and GE1

The AR7241 integrates two Gigabit Ethernet ports that are connected to the Ethernet Switch. The GE0 and GE1 support 2K transmit FIFO and 2K receive FIFO. The WAN port is a MII interface that connects directly to a PHY inside the Ethernet Switch. Another port connects to the Ethernet Switch using a GMII interface. Through the Ethernet Switch this port connects to the four LAN ports. See Figure 2-3.

The AR7241's WAN Ethernet PHY (PHY0) can connect directly to the switch as another port, or can be directly to the CPU through an MII interface.

The PHY interfaces (PHY0, PHY1, PHY2, PHY3 and PHY4) can connect to the switch in bridge mode. In this case GE0 must be under reset. All five LAN ports are switched together and connect to the CPU through the GMII interface (MAC0), which is controlled by the ETH_CFG register bit SW_ONLY_MODE. If GE0 connects separately to PHY, then MAC5 should be under reset.

The GMII and MII MAC interface to the Ethernet Switch support four Tx queues, each with its own descriptor chain. A priority of DMA_TX_Q0 is higher than DMA_TX_Q1 and so on. The DMA configuration registers are separate for each queue. Two arbitration mechanisms are supported: one is a simple priority and the other is a weighted round robin arbitration.

Similarly for rest of the queues. In case of Round robin arbitration on a long term the number of packets sent per queue is guaranteed to be in the ratio of the weights programmed. Weight of ZERO is prohibited. It should be noted that the weights are on a packet basis and not on the number of bytes transmitted on that queue. Moreover, a 19-bit free running counter (running on AHB_CLK) value is updated on the descriptor field as shown below on both the transmit and receive descriptor. This update is done as part of the descriptor update that the MAC DMA core already does upon completion of transmit or receive. Software can track the latency on per packet basis using these descriptor Timestamp and the free timer register.

2.10 MDC/MDIO Interface

The MDC/MDIO interface, which is internal to the AR7241, allows users to access the internal registers of the switch. Table 2-6 shows the format required to access the MII registers in the embedded PHY. The PHY-address is from 0x00 to 0x04. The OP code 10 indicates the read command and 01 indicates the write command.

Table 2-6. **MDC/MDIO Interface Format**

start	Op	2'b0	Phy-addr [2.0]	reg_addr [4:0]	TA [1:0]	Data [15:0]

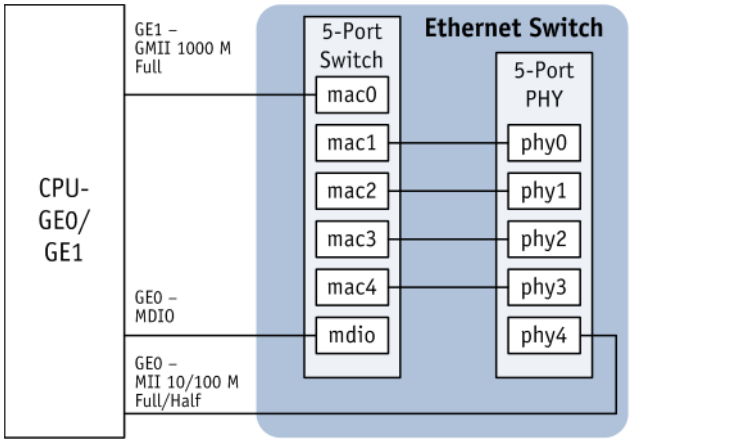
The internal switch registers are 32 bits wide, but MDIO access is only 16 bits wide, so two access cycles are required to access all 32 bits of the internal registers. Address spacing is more than the MDIO-supported 10 bits, thus upper address bits must be written to the internal registers, similar to the page mode access method. For example, register address bits [18:9] are treated as a page address and written out first as High_addr [9:0] (see Table 2-7). Then the register would be accessed via Table 2-6, where Low_addr [7:1] is the register address bit [8:2] and Low_addr [0] is 0 for Data [15:0] or Low_addr [0] is 1 for Data [31:16].

Table 2-7. **Initial Register Address Bits**

start	Op	2'b11	8'b0	6'b0	High_addr [9:0]

2.11 Ethernet Switch Controller

Figure 2-3 shows the Ethernet Switch block diagram.



Notes:
1. mac0 connects to the CPU port and only supports 1000M full duplex mode.
2. phy4 connects to the CPU directly and supports 10/100M full and half duplex.
3. The MDIO interface connects the Ethernet switch to the configuration register.

Figure 2-3. **Ethernet Switch Block Diagram**

The Ethernet Switch controller performs the majority of the switch functions of the AR7241. The controller contains five 10/100 Mbps Fast Ethernet ports, each containing four levels of Quality of Service, 802.1Q VLANs, port based VLANs and RMON statistic counters. The AR7241 integrates five 10/100 two speed Ethernet transceivers (PHYs) and one single port 10/100/1000 media access controllers (MAC) as well as a wire-speed, non-blocking shared memory switch fabric.

The included 1 KB entry address lookup table uses two entries per bucket to avoid hash collisions and maintain packet-forwarding performance. The address entry table provides read/write access from the serial and CPU interfaces where each entry can be configured as a static entry. 1024 MAC addresses are supported with automatic learning, aging and static address support. The Ethernet Switch also supports basic switch features including port mirroring, broadcast storm support, flow control in full-duplex, and back pressure in half duplex, 802.3 auto-negotiation, port locking, MIB counters, ingress and egress rate limitation, and automatic speed and duplex communication between PHYs and MACs.

Table 2-8 summarizes the AR7241 Ethernet Switch functions.

Table 2-8. **Ethernet Switch**

Block	Description
Media Access Controllers (MAC)	The AR7241 integrates six independent fast Ethernet MACs that perform all functions in the IEEE 802.3 and IEEE 802.3u specifications, including frame formatting, frame stripping, CRC checking, CSMA/CD, collision handling, and back-pressure flow control, etc. Each MAC supports 10 Mbps or 100 Mbps operation in either full-duplex or half-duplex mode.
Full-Duplex Flow Control	The AR7241 device supports IEEE 802.3x full-duplex flow control, force-mode full-duplex flow control, and half-duplex back pressure. If the link partner supports auto-negotiation, the 802.3x full-duplex flow control auto-negotiates between the remote node and the AR7241. If full-duplex flow control is enabled, when free buffer space is almost empty, the AR7241 sends out an IEEE 802.3x compliant PAUSE to stop the remote device from sending more frames.
Half-Duplex Flow Control	Half-duplex flow control regulates the remote station to avoid dropping packets during network congestion. A back pressure function is supported for half-duplex operations. When free buffer space is almost empty, the AR7241 device transmits a jam pattern on the port and forces a collision. If the half-duplex flow control mode is not set, the incoming packet is dropped if no buffer space is available.
Inter-Packet Gap (IPG)	The IPG is the idle time between any to successive packets from the same port. The typical IPG is 9.6 µs for 10 Mbps Ethernet and 960 µs for 100 Mbps Fast Ethernet.
Port Locking	The AR7241 supports port locking. If one port is set for port locking, only received frames with the unicast source address found in the ARL table and do not have a member violation, can be sent out. Other blocked frames are dropped or redirected to the CPU port by the control register, LOCK_DROP_EN.
Frame Forwarding Prevention	The AR7240 can be configured to prevent the forwarding of unicast or multicast frames that contain an unknown destination address. This can be accomplished on a per-port basis, so that frames with unknown addresses only go out to the port where a server or router is connected. Broadcast frames forwarded to the CPU port can also be prevented.
Illegal Frames	The AR7240 discards all illegal frames such as CRC error, oversized packets (length greater than maximum length), and runt packets (length less than 64 bytes).
VLANs	See "VLANs For LAN Ports" on page 22.
QoS	See "Quality of Service (QoS) For LAN Ports" on page 23.

2.11.1 VLANs For LAN Ports

The switch supports 16 IEEE 802.1Q VLANs and port-based VLAN functionality for all frames, including management frames when 802.1Q is enabled on the ingress port. Untagged frames conform to the port-based VLAN even if the ingress port has 802.1Q mode enabled. See Table 2-9.

Table 2-9. **Ethernet Switch VLAN**

VLAN	Description
Port-Based	Each ingress port contains a register restricting the output (or egress) ports it can send frames to. This port-based VLAN register has a field called PORT_VID_MEM that contains the port based setting. If bit [0] of PORT_VID_MEM is set to one, the port is allowed to send frames to Port 0, bit [2] for Port 2, and so on. At reset, each port's PORT_VID_MEM is set to a value of all 1s, except for each port's own bit, which clears to zero. Note that the CPU port is port 0.
IEEE 802.1Q VLANs	The AR7241 supports a maximum of 16 entries in the VLAN table. The device supports 4096 VLAN ID range from 0 to 4095. The AR7241 only supports shared VLAN learning (SVL). This means that forwarding decisions are based on the frame's destination MAC address, which should be unique among all VLANs.

Tagging and untagging egress frames is supported using 802.1Q VLANs, or statically using Port Based VLANs. Frames may go out from the switch in three methods:

- Transmit Unmodified
  Untagged frames egress a port untagged while tagged frames leave tagged.
- Transmit Untagged
  Untagged frames leave a port unmodified while tagged frames leave untagged.
- Transmit Tagged
  Tagged frames leave a port unmodified while an IEEE tag is added to untagged frames before leaving.

When a tag is added to an untagged frame, the frame inserts directly after the frame's source address and includes four bytes.

- The first byte is always 0x81.
- The second byte is always 0x00.
- PRI bits indicate frame priority determined by the source port's priority setting.
- The CFI bit is always set to 0.

VID bits indicate the VID assigned to the frame as determined in the source port default VID.

A tagged frame leaving a port tagged may have its VID bits modified. If the ingressing frame's VID was 0x000, the ingress port's default VID is assigned to the frame instead.

Double Tagging is a method of isolating one IEEE 802.1Q VLAN from other IEEE 802.1Q VLANs in a hierarchical fashion that is compatible with IEEE 802.1Q ready switches, as long as those switches support a maximum frame size of 1526 bytes or more. In this way, an extra, or double, tag is placed in front of a frame's normal tag thereby increasing the frame's size by four bytes.

Ingress double tagging can be selected on a port-by-port basis. Typically, any port that has ingress double tagging enabled will also have egress double tagging enabled. Ingress double tagging enabled ports expect all ingress frames to contain an extra tag that must be removed from the frame before performing the port's ingress policy on the frame. In this mode, the ingress policy removes the first IEEE 802.3ac tag that appears after the source address in every frame. If the untagged frame is not modified, all data from the removed tags is ignored by the switch.

2.11.2 Quality of Service (QoS) For LAN Ports

The AR7241 recognizes the QoS information of ingress frames and map to different egress priority levels. The AR7241 determines the priority of the frames based on DA, TOS/TC, VLAN, and port. Each has an enable bit that can be applied. When more than one type of priority is selected, the order in which the frame priority should be applied can be determined. Priority enable bits and select order bits are set by port base at 0x110 for port 0, 0x210 for port 1, and so on.

Priority Determined	Description
DA	Set DA_PRI_EN bit [18] to 1 and add the address to the ARL table-set priority_over_en to 1. ARL priority bits [59:58] can be used as DA priority.
ToS/TC	Set IP_PRI_EN bit [16] to 1, and set the IP priority mapping register (0x60–0x6C).
VLAN	Set VLAN_PRI_EN (bit [17]) to 1, and set the TAG priority mapping register (0x70).
Port's Default Authority	Set PORT_PRI_EN to 1, and set port base register ING_PORT_PRIORITY (bits [19:28] in 0x108, 0x208, etc.).

When more than one priority enable bit is set to 1, bits [7:0] in 0x110, 0x210, etc. (DA_PRI_SEL, IP_PRI_SEL, VLAN_PRI_SEL, PORT_PRI_SEL) can determine the order in which the frame priority should be applied. If *_PRI_SEL is set to 00, frame priority is determined by that first. Otherwise, priority is determined by which *_PRI_SEL is set to 01, then 10, 11, etc.

On arrival, packets are directed into one of the four available priority queues based on:

- Priority bits in the header field
- The frame destination address (if in the ARL table with a defined priority with the priority bit is enabled)
- The frame VID (if in the VLAN table and the priority override is enabled)
- The 802.3 tag containing 802.1p priority information (if enabled on the port)
- The port's default priority as defined in the register

Each of the priority classification rules have enables so designers may use any combination; priority can be disabled or the order may be selected separately on a per-port basis.

Congestion in the flow of packets for an extended period of time forces frames to drop without flow control. Higher priority flows receive a higher percentage of the open buffers, and this percentage is determined by the scheduling mode. Features such as back pressure and pause-frame control are implemented to supports zero packet loss during traffic congestion. The AR7241 ensures that all uncongested flows traverse the switch without degradation, regardless od congestion situations elsewhere in the switch.

QoS for the AR7241 may follow one of three priority schemes, either fixed, weighted fair, or a mixed mode scheme. In the fixed priority scheme, all egress packets leave the switch starting with the highest priority queue. Once that queue has been emptied, the next highest priority queue begins its packet dispersal until it has been emptied and so on. This method insures that all high priority packets will be sent out from the switch as soon as possible.

For the weighted fair scheme, packets are egressed from the chip in the order of 8, 4, 2, 1 packets for the four priorities queue of the AR7241. (eight packets egress from the highest priority queue, then four from the second highest queue, and so on). This method allows the highest priority to get its packets out first and the other remaining queues are not totally starved from egressing.

The mixed mode scheme mixes both the weighted fair and fixed schemes. The highest priority queue disperses its packets first until the queue has been emptied, and the remaining queues will follow the 4, 2, 1 weighted egress scheme as mentioned previously. This ensures that the highest priority queue will egress its packets as soon as possible, while the remaining queues equally disperse their packets without queue starvation.

2.12 Rate Limiting

The AR7241 supports port-based ingress and egress rate limiting. All frames may be limited but management frames and known multicast frames are the only types that can be selected by the user. The ingress limit rate may be set from zero to 1 Gbps in steps of 32 Kbps. The port base register is used to determine the limited bytes to count. The default setting for rate limiting is to include the frame's bytes from the beginning of the preamble to the end of the RCS with a added minimum IFG.

2.13 Broadcast Storm Control

The AR7241 supports broadcast storm control. Some switch designs may require limiting the reception rate of frames. The types of frames to be limited can be selected separately on a per-port basis.The maximum rate desired needs to be selected by the user and then programmed. Eleven different frame rates from 1k (2^0K) to 2^{10}K per second.

The statistics counter block maintains a set of forty MIB counters per port. These counters provide a set of Ethernet statistics for frames received on ingress and transmitted on egress. A register interface allows the CPU to capture, read, or clear the counter values.

The counters support:

- RMON MIB
- Ethernet-like MIB
- MIB II
- Bridge MIB
- RFC2819

The CPU interface supports:

- Autocast MIB counters after half-full
- Autocast MIB counters after time out
- Autocast MIB counters when requested
- Clearing all MIB counters

The MIB counters in the switch are for LAN's and CPU port. For WAN, the MIB counters are in GE1.

2.14 Switch Operation

Two tables embedded in the AR7241 aid in allocation of ingress packets, the ARL table and the VLAN table.

The address database is stored in the embedded SRAM and can store up to 1024 address entries. The default aging time for this table is 300 seconds. One address can be searched in the table and it may be used to get the next read out of the whole table. Entries in the table may be loaded and purged. All entries maybe be flushed, and this may be divided to flush just non-static entries, all entries per port or all non-static entries per port.

The VLAN table supports a single search, and it may be used to get the next read out of the whole table. Entries may be loaded or purged and entries may be flushed, either as a whole or per port.

2.15 Port Mirroring

Ingress, egress and destination address packets can be mirrored by the AR7241. To mirror the DA packets, the mirror enable bit must be set in the ARL table. To mirror a port, simply set the mirror port number.

Port mirroring is only among the LAN ports and not for WAN.

2.16 Port States

Table 2-10 shows the port states supported by the AR7241.

Table 2-10. **Port States**

State	Description
Disabled	Frames are not allowed to enter or leave a disabled port. Learning does not take place on disabled ports.
Blocking	Only MGMP frames are allowed to enter a blocked port. All other frame types are discarded. Learning is disabled on blocked ports.
Listening	Only management frames may enter or leave a listening port. All other frame types are discarded. Learning is disabled on listening ports.
Learning	Only management frames may enter or leave a learning port. All other frame types are discarded but learning occurs on all good frames, including non-management frames.
Forwarding	Normal operation. All frames may enter or leave a forwarding port. Learning occurs on all good frames.

3. Audio Interface

3.1 Overview

Figure 3-1 shows a block diagram of the AR7241 audio interface.

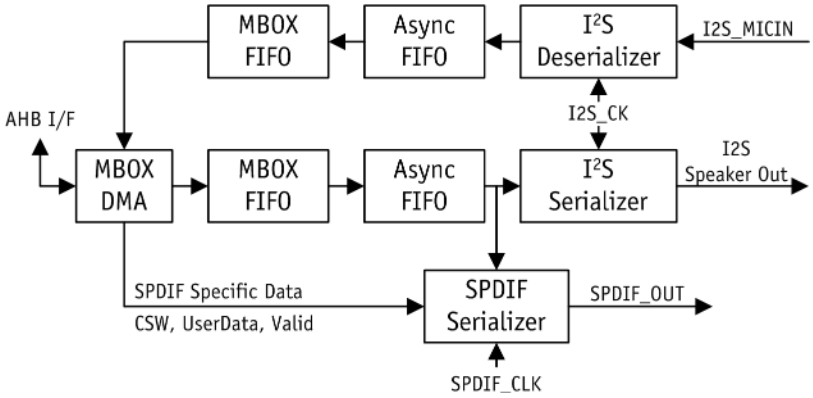


Figure 3-1. **Audio Interface**

The AR7241 includes an I²S speaker and microphone interface as well as an SPDIF speaker interface. The I²S and SPDIF clocks are generated by the audio PLL block.

3.2 Audio PLL

Figure 3-2 shows the AR7241 audio PLL block diagram.

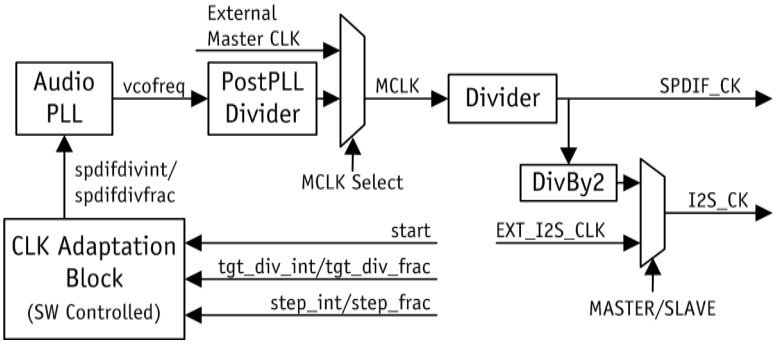


Figure 3-2. **Audio PLL Block Diagram**

The audio PLL can support generation of all the audio master clock frequencies. It accepts two inputs, SPDIFDIVINT and SPDIFDIVFRAC, which are generated by a clock adaptation module. The clock adaptation module enables slow changing of the audio clock by changing SPDIFDIVINT/ SPDIFDIVFRAC in small steps from the current value to a target value. The target TGT_DIV_INT/TGT_DIV_FRAC and step size are software programmable. The clock adaptation module changes the value of the SPDIFDIVINT/SPDIFDIVFRAC values with respect to a slow SPDIFCLKSDM clocks. This small step size ensures that the audio PLL tracks the small variation. The resolution of DIVFRAC ensures that the clock can be varied with steps less than 200 ppb. Following the audio PLL come three dividers: postPLL divider and ExtDiv controlled through the register AUDIO_PLL_CONFIG, PostPLLDivide field, and another posedge divider inside the I²S STEREO_CONFIG register. The final clock relations is:

(40 MHz/3) * (int.frac) = vcofreq
vcofreq/(PostPLLDiv * ExtDiv) = MCLK
MCLK/posedge = SPDIF_CLK

If the master must be modified from the current value to another value, it is software's responsibility to recompute and program the new TGT_DIV_INT/TGT_DIV_FRAC values.

3.3 I²S Interface

The AR7241 I²S supports a two-channel digital audio subsystem. This interface uses the I²S pins listed in Table 1-2, "Signal-to-Pin Relationships and Descriptions," on page 8.

3.3.1 External DAC

An external DAC receives I²S digital audio streams and converts them to analog output to drive speaker or headphones. This data stream is PCM data which is serialized and sent with a left channel/right channel select and synchronization signal. The I²S serializer can be programmed to support a few different variants of the I²S data format to be compatible with a larger number of external DAC components, including various PCM data word sizes, serialization boundaries, and clocking options.

I²S can also operate in a slave mode where the stereo clock and word select are driven by external master (DAC or external controller). External DAC parts are often controlled by a separate serial 2-wire or 3-wire interface. This interface often controls volume and configuration of the external DAC. This can be attached to the AR7241 serial interface controllers.

3.3.2 Sample Sizes and Rates

The stereo audio path supports PCM sample sizes of 8, 16, 24, or 32 bits for speaker out and PCM sample sizes of 16 and 32 bits for MICIN. The serializer supports serialization sizes of 16 or 32 bits. The sample size and serialization size need not be the same, LSBs will be padded with 0's. If the AR7241 is programmed to be a slave, word select and stereo clock (the bit clock) are inputs from the external DAC/ADC.

Along with configuration information, a sample counter provides the number of samples transmitted per second through the I²S SpeakerOut interface. This sample counter can be used and cleared by software as required.

3.3.3 Stereo Software Interface

To play music, software configures the stereo subsystem and sends interleaved (LRLR....) PCM data to the mailbox DMA. To record music, software configures the stereo subsystem and the PCM samples (interleaved) are written into the memory.

To send data PCM samples on the I²S interface:

1. Configure other parameters.
   For example, sample size, word size, mono/stereo mode, master/slave mode, clk divider (if the AR7241 is master), and so on.
2. Program GPIO_FUNCTION register to enable I²S.
3. Program the STEREO_CONFIG register to enable the stereo.
4. Issue a stereo reset.
5. Configure the DMA to send SpeakerOut from the AR7241.

To receive data PCM samples:

1. Program the GPIO_FUNCTION register to enable I²S.
2. Program STEREO_CONFIG register to enable the stereo.
3. Issue a MICIN reset to reset Micin buffers.
4. Configure other parameters.
   For example, sample size, word size, mono/stereo mode, master/slave mode, clk divider (if the AR7241 is master), and so on.
5. Configure the DMA to receive PCM samples.

3.4 SPDIF INTERFACE

The AR7241 also includes a SPDIF interface for audio. The SPDIF interface only includes SPDIF_OUT to the speakers. SPDIF_IN is not supported in the AR7241.

The SPDIF interface operates on the same sample as I²S, so it always in sync with audio played on the I²S interface. All configuration information to the SPDIF block, such as the sampling frequency, sample size, word size, and so on, are inherited from the programming of the I²S interface. If only the SPDIF interface is required to operate and the I²S audio interface is not required, the programming still only needs to be done using I²S configuration registers. The I²S interface can be disabled using the GPIO function register.

The SPDIF specific data that forms part of each SPDIF audio subframe such as the valid, CSW, and user data are provided through the DMA descriptor directly to the SPDIF Module. The DMA controller describes how the data is provided through the descriptor.

3.5 MAILBOX (DMA CONTROLLER)

A MBOX DMA Controller is used in the AR7241 for I^2S and SPDIF interface. The MBOX channel is a duplex channel that can operate simultaneously for Rx and Tx.

3.5.1 Mailboxes

The AR7241 supports one duplex mailbox to move data between the DDR memory and audio interfaces I^2S and SPDIF through the AHB interface. Flow control of the DMA must be managed by software.

3.5.2 MBOX DMA Operation

The AR7241 MBOX DMA engine has one channel for Tx and one channel for Rx. Each mailbox DMA channel follows a list of linked descriptors.

Figure 3-3 and Table 3-1 show the descriptor format and description.

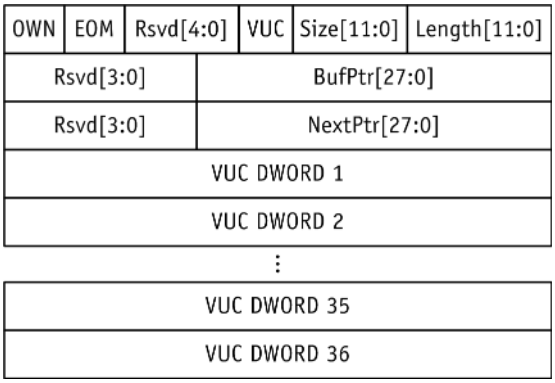


Figure 3-3. **DMA Descriptor Structure**

Table 3-1. **Descriptor Fields**

Name	Bits	Description
Length	12	Length of data in memory buffer. If EOM=0, the Length = Size.
Size	12	Size of memory buffer.
VUC	1	When this bit set, the SPDIF block uses the VUC data for the audio block fetched from the previous descriptor.
EOM	1	End of message indicator.
OWN	1	Descriptor is owned by the CPU or DMA engine. (If set, it is owned by the DMA engine).
BufPtr	28	Points to memory buffer pointer. Byte aligned address.
NextPtr	28	Points to next descriptor in the list. Must be word aligned.
VUC DWORD 1 to 36	36 * 32 bits	These are the VUC data for each audio block of the SPDIF. 192 Bits each of Valid, UserData and Channel Status Word for two channels of audio corresponds to 36 Dwords. These data are SPDIF specific and software does not need to provide this data if I^2S is the only active interface and SPDIF is disabled.

Once the DMA engine is started, it will follow its descriptor chain until it arrives at a descriptor that has its owner bit set to CPU (bit [31] of the status word is not set). The DMA engine then stops until the CPU restarts it.

The DMA control registers include stop and start commands, a programmable descriptor chain base address, DMA policies to use, and so on. DMA status registers inform the CPU when the engine is running, done, or encountered an error.

3.5.3 Software Flow Control

To configure the MBOX channel to send data from the AR7241 (Rx as referred in MBOX):

1. Set up the MBOX Rx descriptors. The owner should be set to indicate it is owned by the DMA controller. Hardware resets this once DMA is complete.
2. Load the corresponding buffers with the data to transmit.
3. Program the register MBOX_DMA_TX_DESCRIPTOR_BASE_ADDRESS with the base descriptor address.
4. Reset the corresponding MBOX FIFO.
5. Enable the DMA by setting the START bit in the MBOX_DMA_RX_CONTROL register. This register has a provision to stop and resume at any time.
6. On DMA completion, the RX_DMA_COMPLETE interrupt is asserted.

To configure the MBOX channel for the AR7241 to receive data (Tx as referred in MBOX):

1. Set up the MBOX Tx descriptors. The owner should be set to indicate it is owned by the DMA controller. Hardware resets this once DMA is complete.
2. Program the register MBOX_DMA_TX_DESCRIPTOR_BASE_ADDRESS with the base descriptor address.
3. Reset the corresponding MBOX FIFO.
4. Enable the DMA by setting START bit in MBOX_DMA_TX_CONTROL register. This register has a provision to stop and resume at any time.
5. On DMA completion, the TX_DMA_COMPLETE interrupt is asserted.

3.5.4 Mailbox Error Conditions

If flow control synchronization is lost for any reason, these mailbox error conditions could arise:

Tx Mailbox Overflow	If no DMA descriptors are available on the AR7241 Tx side, but an message is coming in from the corresponding interface, the Tx mailbox stalls the host physical interface. If the host interface remains stalled with the Tx FIFO full for a timeout period specified other than FIFO_TIMEOUT, a timeout error occurs. An interrupt is sent to CPU. As long as the host status overflow bit is set, any mailbox Tx bytes that arrive from the host when the mailbox is full are discarded. When the host clears the overflow interrupt, mailbox FIFOs return to normal operation. Software must then either resynchronize flow control state or reset the AR7241 to recover.
Rx Mailbox Underflow	If I^2S reads a mailbox that does not contain any data and this condition persists for more than a timeout period, the CPU is sent an underflow error interrupt. As long as status underflow bit is set, any mailbox reads which arrive when the mailbox is empty return garbage data. Software must then either resynchronize flow control state or reset the AR7241 to recover.

3.5.5 MBOX-Specific Interrupts

All MBOX specific interrupts can be masked by control registers (MBOX_INT_ENABLE).

MBOX sends an interrupt to MIPS in these cases (if they are enabled):

- Tx DMA complete, Rx DMA complete
- Tx overflow, Tx not empty (incoming traffic)
- Rx underflow, Rx not full (outgoing traffic)

The status of these interrupts can be read from the MBOX_INT_STATUS register.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 summarizes the absolute maximum ratings and Table 4-2 lists the recommended operating conditions for the AR7241.

Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 4-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max Rating	Unit
V_{dd12}	Supply voltage	–0.3 to 1.8	V
V_{dd25}	Maximum I/O supply voltage	–0.3 to 4.0	V
T_{store}	Storage temperature	–65 to 150	°C
T_j	Junction temperature	TBD	°C
ESD	Electrostatic discharge tolerance	2000	V

4.2 Recommended Operating Conditions

Table 4-2. **Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD33}	Supply Voltage	±10%	2.97	3.3	3.63	V
V_{DD25}	I/O Supply Voltage[1]	±5%	2.49	2.62	2.75	V
V_{DD12}	Core Voltage[1]	±5%	1.14	1.2	1.26	V
V_{DD12CD}	Core Voltage for CPU/DDR[1]	±5%	1.22	1.28	1.34	V
AV_{DD20}	Voltage for Ethernet PHY[1]	—	1.9	2.0	2.15	V
V_{DD_DDR}	DDR1 I/O Voltage[1]	±5%	2.47	2.6	2.73	V
	DDR2 I/O Voltage[1]	±5%	1.71	1.8	1.89	1.71
D_{DR_VREF}	DDR1 Reference Level for SSTL Signals[2]	—	1.24	1.3	1.37	V
	DDR2 Reference Level for SSTL Signals[2]	—	0.86	0.9	0.95	V
T_{case}	Case Temperature	—	—	—	TBD	°C
Psi_{JT}	Thermal Parameter[3]	—	—	—	3.1	°C/W

[1]Voltage regulated internally by the AR7241
[2]Divide VDD_DDR voltage by two externally, see reference design schematic
[3]The thermal parameter is for the 14x14 mm LQFP package.

4.3 General DC Electrical Characteristics

Table 4-3 lists the general DC electrical characteristics.

These conditions apply to all I/O DC characteristics unless otherwise specified:

T_{amb} = 25 °C, V_{DD25} = 2.62 V

Table 4-3. **General DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	2.0	—	2.8	V
V_{IL}	Low Level Input Voltage	—	–0.3	—	0.4	V
I_{IL}	Input Leakage Current	With pull down	—	26	—	µA
V_{OH}	High Level Output Voltage	I_o = 1 mA	2.2	—	2.8	V
V_{OL}	Low Level Output Voltage	I_o = 1 mA	0	—	0.4	V
I_O	Output Current	V_o = 0 to V_{dd}	—	1	—	mA
	GPO_13 to GPO_17 when used as LED_0 to LED_4	V_o = 0 to V_{dd}	—	10	—	mA
C_{IN}	Input Capacitance	—	—	3	—	pF

Table 4-4 lists the DDR1 DC electrical characteristics:

T_{amb} = 25 °C, V_{DD_DDR} = 2.6 V

Table 4-4. **DDR1 Interface DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	1.48	—	2.9	V
V_{IL}	Low Level Input Voltage	—	–0.3	—	1.12	V
V_{OH}	High Level Output Voltage	I_o = 1 mA	2.2	—	2.8	V
V_{OL}	Low Level Output Voltage	I_o = 1 mA	–0.3	—	0.4	V

Table 4-5 lists the DDR2 DC electrical characteristics:

T_{amb} = 25 °C, V_{DD_DDR} = 1.8 V

Table 4-5. **DDR2 Interface DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	1.1	—	2.2	V
V_{IL}	Low Level Input Voltage	—	–0.3	—	0.8	V
V_{OH}	High Level Output Voltage	I_o = 1 mA	1.6	—	2.2	V
V_{OL}	Low Level Output Voltage	I_o = 1 mA	–0.3	—	0.4	V

Table 4-6 lists the EJTAG and LDO DC electrical characteristics:

T_{amb} = 25 °C, V_{DD25} = 2.62 V

Table 4-6. **EJTAG and LDO DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage (EJTAG_SEL, TRST_L, TCK, LDO_DDR_SEL)	—	2	—	3.6	V
V_{IL}	Low Level Input Voltage (EJTAG_SEL, TRST_L, TCK, LDO_DDR_SEL)	—	–0.3	—	0.4	V
V_{IH}	High Level Input Voltage (TMS, TDI)	—	2	—	2.8	V
V_{IL}	Low Level Input Voltage (TMS, TDI)	—	–0.3	—	0.4	V
V_{OH}	High Level Output Voltage (TDO)	—	2.2	—	2.8	V
V_{OL}	Low Level Output Voltage (TDO)	—	0	—	0.4	V

4.4 40 MHz Clock Characteristics

The 40 MHz reference clock can be AC coupled sine wave or square wave. An external 100 pF capacitor should connect between REFCLKIN and the clock source. See Table 4-7 and Table 4-8 for more information.

Table 4-7. **40 MHz Clock Sine Wave Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{Ampl}	Peak-to-Peak Amplitude	—	0.6	—	1.4	V

Table 4-8. **40 MHz Clock SquareWave Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{Ampl}	Peak-to-Peak Amplitude	—	0.6	—	1.2	V
T_{DCycle}	Duty Cycle	—	40	50	60	%
T_{Rise}	Rise Time	—	—	—	3	ns
T_{Fall}	Fall Time	—	—	—	3	ns

4.5 Power Consumption

Primary voltage supply of the AR7241 is provided by the VDD33, pins 71 and 117. The VDD33 is regulated by the internal LDOs to supply power to the external DDR memory, and magnetics of the Ethernet ports.

Figure 4-1 depicts the AR7241 power consumption. Refer to the reference design schematics for details. Table 4-9 shows the typical power consumption for the AR7241 with internal 5-port Ethernet Switch, PCIE interface in operating mode.

Table 4-9. **Power Consumption**

Symbol	Voltage (V)	Current (mA)
V_{DD33}	3.3	TBD

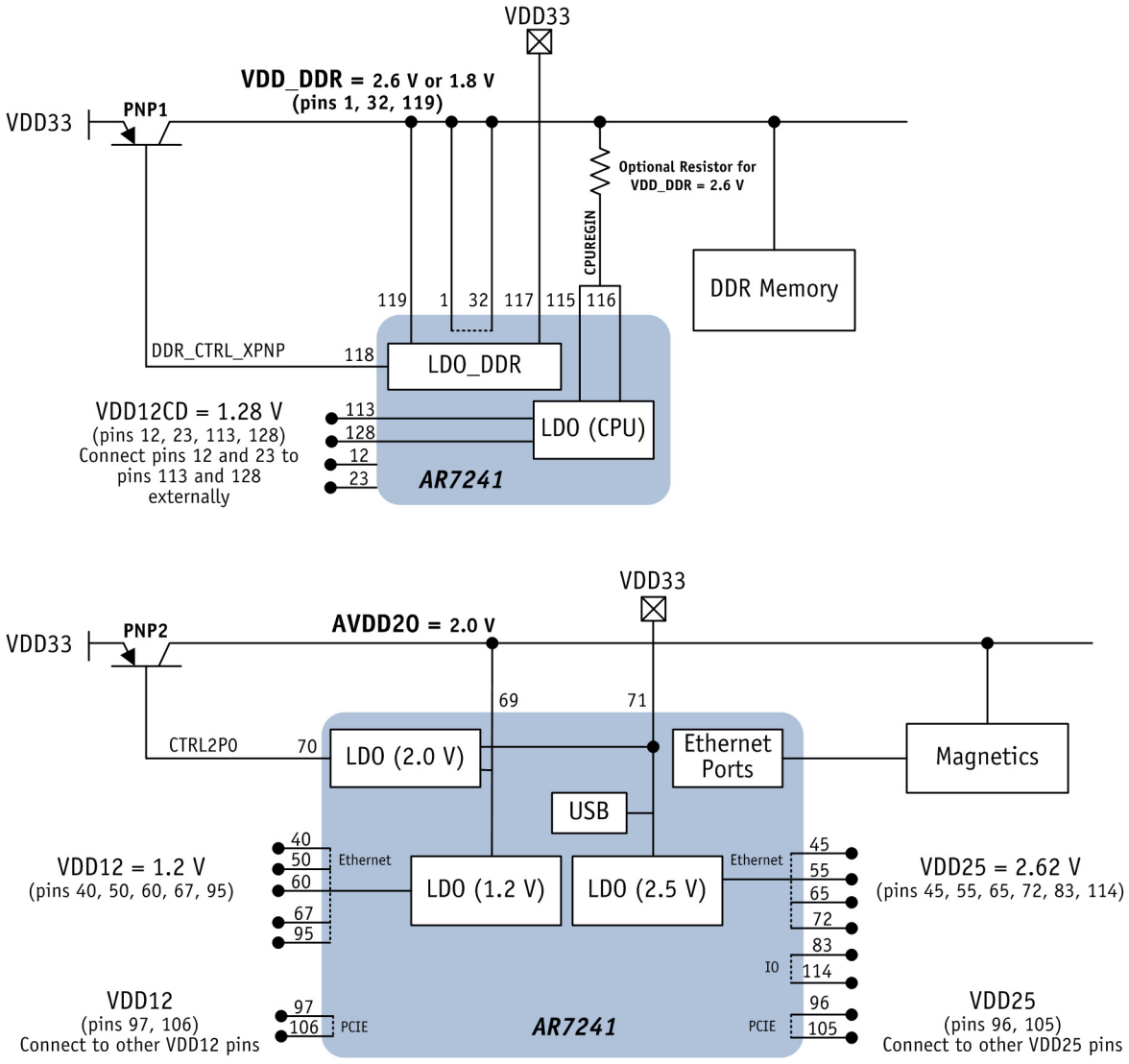


Figure 4-1. **Output Voltages Regulated by the AR7241**

5. Package Dimensions

The AR7241 14 mm x 14 mm LQFP-128 package drawings and dimensions are provided in Figure 5-1, Table 5-1, and Table 5-2.

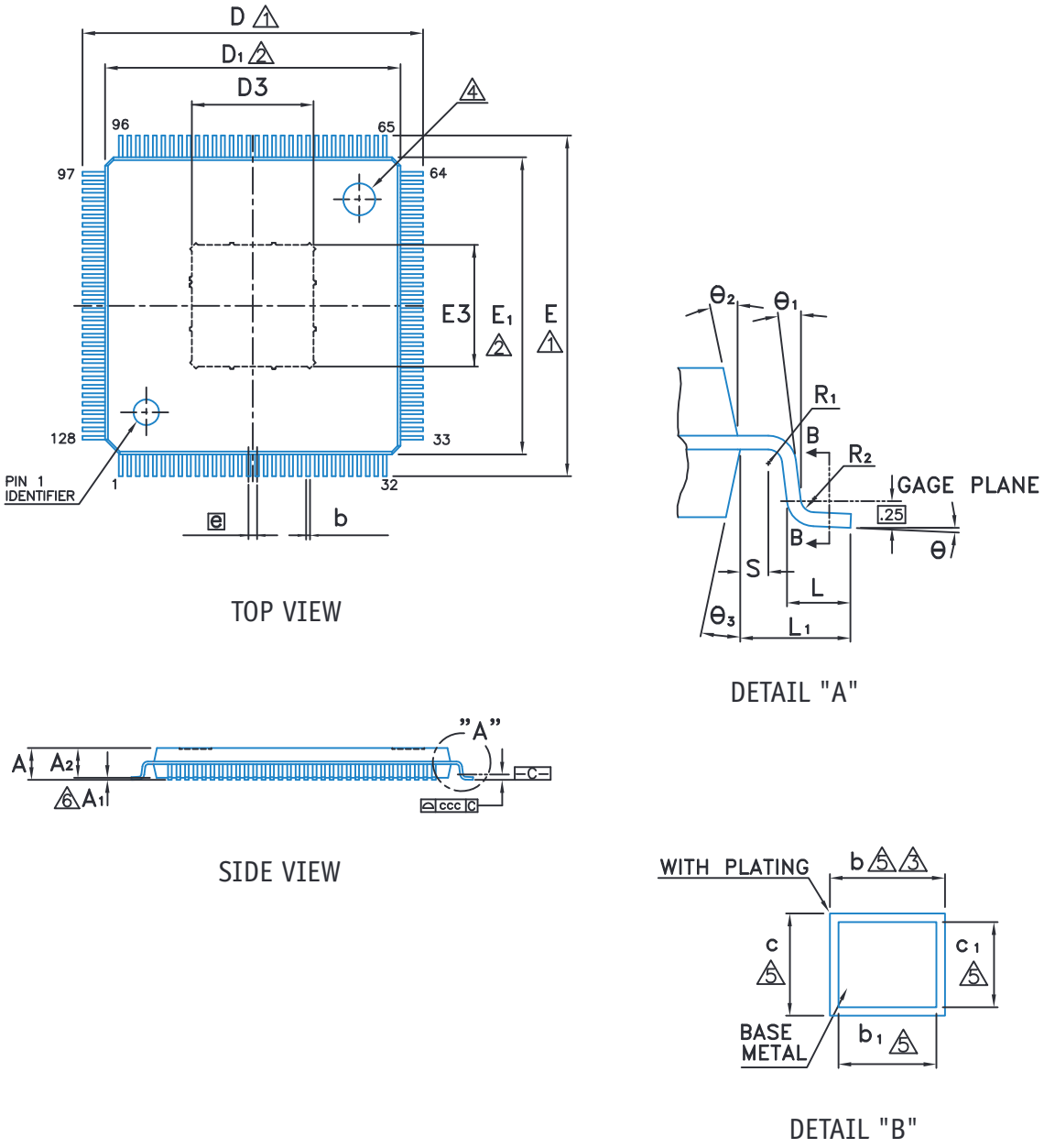


Figure 5-1. **Package Details**

Table 5-1. **Package Dimensions**

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	—	—	1.60	mm	—	—	0.063	inches
A1	0.05	—	—	mm	0.002	—	—	inches
A2	1.35	1.40	1.45	mm	0.053	0.055	0.057	inches
b	0.13	0.18	0.23	mm	0.005	0.007	0.009	inches
b1	0.13	0.16	0.19	mm	0.005	0.006	0.007	inches
c	0.09	—	0.20	mm	0.004	—	0.008	inches
c1	0.09	—	0.16	mm	0.004	—	0.006	inches
D	15.85	16.00	16.15	mm	0.624	0.630	0.636	inches
D1	13.90	14.00	14.10	mm	0.547	0.551	0.555	inches
E	15.85	16.00	16.15	mm	0.624	0.630	0.636	inches
E1	13.90	14.00	14.10	mm	0.547	0.551	0.555	inches
e		0.40 BSC		mm		0.016 BSC		inches
L	0.45	0.60	0.75	mm	0.018	0.024	0.030	inches
L1		1.00 REF		mm		0.039 REF		inches
R1	0.08	—	—	mm	0.003	—	—	inches
R2	0.08	—	0.20	mm	0.003	—	0.008	inches
S	0.20	—	—	mm	0.008	—	—	inches
θ	0	3.5	7	°	0	3.5	7	°
θ1	0	—	—	°	0	—	—	°
θ2/θ3		12° TYP				12° TYP		
ccc		0.08		mm		0.003		inches

[1] To be determined at seating plane C.
[2] Dimensions D1 and E1 do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
[3] Dimension b does not include dambar protrusion. Dambar cannot be located on the lower radius of the foot.
[4] Exact shape of each corner is optional.
[5] These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
[6] A1 is defined as the distance from the seating plane to the lowest point of the package body.
[7] Controlling dimension: Millimeters
[8] Reference document: JEDEC MS-026.
[9] Special characteristics C class: ccc.

Table 5-2. **Exposed Pad Size**

L/F	Dimension	Unit	Dimension	Unit
D3/E3	5.72/5.46 REF	mm	0.225/0.215 REF	inches

6. Ordering Information

The order number AR7241-AH1A specifies a LQFP halogen-free standard-temperature version of the AR7241.

Document Number: 981-00097-001 MKG-1154 Rev. 1

Atheros Communications, Incorporated
5480 Great America Parkway
Santa Clara, CA 95054
t: 408/773-5200
f: 408/773-9940
www.atheros.com